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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/549,865	07/28/2006	Victor Higgs	427008037US	4772
34036 7590 05/27/2008 Silicon Valley Patent Group LLP			EXAMINER	
18805 Cox Avenue			AKANBI, ISIAKA O	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Application No. Applicant(s) 10/549.865 HIGGS, VICTOR Office Action Summary Examiner Art Unit ISIAKA O. AKANBI 2886 -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS. WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status 1) Responsive to communication(s) filed on 28 July 2006. 2a) This action is FINAL. 2b) This action is non-final. 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims 4) Claim(s) 1-19 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) _____ is/are allowed. 6) Claim(s) 1-9 and 14-19 is/are rejected. 7) Claim(s) 10-13 is/are objected to. 8) Claim(s) _____ are subject to restriction and/or election requirement. Application Papers 9) The specification is objected to by the Examiner. 10) ☐ The drawing(s) filed on 22 September 2005 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. Priority under 35 U.S.C. § 119 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.

1) Notice of References Cited (PTO-892)

Notice of Draftsperson's Patent Drawing Review (PTO-948)
Notice of Draftsperson's Patent Drawing Review (PTO-948)
Notice of Draftsperson's Patent Drawing Review (PTO-948)

Paper No(s)/Mail Date 08 January 2008 and 13 February 2008.

Attachment(s)

Interview Summary (PTO-413)
Paper No(s)/Mail Date.

6) Other:

5) Notice of Informal Patent Application



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DETAILED ACTION

Preliminary Amendment

The preliminary amendment filed on 22 September 2005 has been entered into this application.

Information Disclosure Statement

The information disclosure statement filed on 08 January 2008 and 13 February 2008 has been entered and considered by the examiner.

Drawings

The drawings filed on 22 September 2005, has been accepted for examination.

Claim Objections

Claims 10, 11, 12 and 13 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim should refer to other claims in the alternative only and/or cannot depend from any other multiple dependent claim. See MPEP § 608.01(n). Accordingly, the claims have not been further treated on the merits.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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Claims 1-9 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Higgs (WO 02/29883 A1).

Regarding claims 1 and 14, Higgs discloses a method of detecting surface particulate defects, and especially metal particulates, in semiconductors such as silicon, to characterise defects likely to have an effect on the electrical activity of such semiconductor materials, comprises the steps of:

exposing the surface of the semiconductor structure in the vicinity of a surface particulate to at least one high-intensity beam of light from a suitable light source (fig. 5: 3-8)([pars. 0045-0046]);

collecting photoluminescence produced by excitation of the semiconductor structure by the light beam (see, abstract, [pars. 0012, 0037, 0058] and page 20, lines 7-9);

processing/analyzing (the signal) the collected photoluminescence to produce a result representative of the intensity of the photoluminescence response (fig. 5: 40)([pars. 0062], page 20, lines 9-11);

Higgs further discloses inspecting (to examine carefully and critically, to examine (two or more objects, ideas, people, etc.) in order to note similarities and differences, especially for flaws) the map for one or more regions of enhanced PL intensity, identifying characteristic (near) surface metal contamination; and inspecting for one or more regions of enhanced PL intensity identifying potential front side or back side diffusable metal contamination; and verifying by additional tests (See abstract,

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lines 6-9, [pars. 0012, 0037] page 20, lines 9-11 and page 22, lines 26-28), and thus meet the limitation comparing (to examine) the result with a predetermined acceptable specification range of photoluminescence to identify unacceptable contamination levels resulting from diffusion of contaminant from particulate into semiconductor structure.

As to claim 2, Higgs also discloses inspecting (to examine carefully and critically, to examine (two or more objects, ideas, etc.) in order to note similarities and differences, especially for flaws) the map for one or more regions of enhanced PL intensity, identifying characteristic (near) surface metal contamination (See abstract, lines 6-9, [pars. 0012, 0037] page 20, lines 9-11 and page 22, lines 26-28); Higgs further discloses that use of the equipment enables localisation and characterisation of certain PL characteristic metal contaminants in semiconductors ([par. 0064, screen= to select, reject, consider, or group (people, objects, ideas, etc.) by examining systematically]); which is a systematic grouping of semiconductor or silicon structure based on the analysis and thus constitutes a quality classification of the semiconductor structure based upon such a comparison, and rejecting or selecting for remedial action semiconductor structures exhibiting a photoluminescence response outside the said predetermined acceptable specification range.

As to claim 3, Higgs also discloses using yield test to determined device performance and reliability (page 1, [par. 0002]), and thus meet the limitations a prior step of determining a predetermined acceptable specification from studies of samples of fabricated devices using electrical yield test methods.

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As to claims 4 and 5, Higgs also discloses wafers were excited using laser excitation (to increase the energy (i.e. heat or power of semiconductor) and contaminated, and then the levels of contamination is confirmed, detected or determined for different images (figs. 1-4)(page 17, [pars, 0067-0069]), and thus meet the limitations wherein the semiconductor is annealed prior to carrying out the detection steps to diffuse contaminant from the particle into the semiconductor material and make detection easier and wherein the detection steps are repeated prior to and subsequent to an annealing step and the results compared to determine the difference and obtain an indication of rates of diffusion so as to identify the contaminant.

As to claims 6 and 7, Higgs also discloses a method of detecting surface particulate defects, and especially metal particulates, in semiconductors such as silicon, to characterise defects likely to have an effect on the electrical activity of such semiconductor materials. comprises:

a first step of collecting photoluminescence by:

exposing the surface of the semiconductor structure in the vicinity of a surface particulate to at least one high-intensity beam of light from a suitable light source (i.e. Laser)(page 21, lines 14-15)(fig. 5: 3-8)([pars. 0012, 0037, 0045-0046]);

collecting photoluminescence produced by excitation of the semiconductor structure by the light beam (see abstract, lines 4-6)([pars. 0012, 0037, 0045-0046]);

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processing/analyzing (the signal) the collected photoluminescence to produce a first photoluminescence result representative of the intensity of the photoluminescence response (fig. 5: 40)([pars. 0062], page 20, lines 9-11);

Higgs further discloses exposing the semiconductor or contaminated silicon wafers to excitation beam, producing a image mapping the location of the particulates as a dark field image of light scattered from the surface the semiconductor structure (figs. 1-5) and collecting luminescence (after excitation=second step) from the structure in the form of a PL map and inspecting (to examine carefully and critically, to examine (two or more objects, ideas, people, etc.) in order to note similarities and differences between contaminated and the control semiconductor, especially for flaws) for one or more regions of enhanced PL intensity identifying potential front side or back side diffusable metal contamination (pars. 0016, 0037, 0064-0068); and thus meet the limitations such as a heating step to the semiconductor to diffuse contaminant from the particle into the semiconductor material; a second step of collecting photoluminescence produced by like method to the first to produce a second photoluminescence result representative of the intensity of the photoluminescence response as above described after annealing; a step of comparing the results of each photoluminescence step to determine the difference and obtain an indication of rates of diffusion so as to identify the contaminant.

As to claims 8 and 9, Higgs discloses the limitations wherein the spatial resolution of the laser is 0.1 to 20 µm (page 21, lines 26-27); wherein the laser provides a peak or average power density of between 10⁴ to 10⁹ watts/cm² (page 22, lines 4-7)

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and wherein the light beam used to generate the PL effect is so controlled as to Collect PL information from no deeper than the upper (i.e. 12 µm) of the semiconductor structure (page 22, lines 1-2)([par. 0033-0034]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior at are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higgs (WO 02/29883 A1) in view of Noguchi et al. (6,730,594 B2).

As to claims 15 and 17, Higgs teaches excitation of a semiconductor which is a process of increasing the energy (i.e. heat or power) of semiconductor.

Higgs fails to explicitly specify a means to heat the sample under test is associated with the support or the heating means comprises a heated stage.

However, using a measuring stage or support that is associated with heating means is common and know in the art, as evidenced by Noguchi (fig. 4: H) (col. 8, lines 27-32).

Therefore it would have been at least obvious to one having ordinary skill in the art at the time of invention to modify Higgs by associated a heating means with the

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support or a heating means comprising a heated stage for the purpose of controlling the temperature of the sample with accuracy, as per the teachings of Noquchi.

As to claim 16, Higgs teaches of an apparatus for detecting surface particulate defects, and especially metal particulates, in semiconductors such as silicon, to characterise defects likely to have an effect on the electrical activity of such semiconductor materials, comorises:

a high intensity light source (fig. 5: 3-8)([pars. 0045-0046]);;

means (fig. 5: 30 and 34) to focus a high intensity beam of light from the light source onto a surface of a semiconductor sample under test on the support ([par. 0048]);;

collection means (fig. 5: 14, 34, 31) to collect photoluminescence data produced by excitation of the semiconductor structure by the light beam at least in the vicinity of particulates on the surface (fig. 5: 2) thereof;

means (fig. 5: 25 and 29) to process the collected data to produce a result representative of the intensity of the photoluminescence response in the said vicinity ([pars. 0050-51]);

a microprocessor (fig. 5: 40) includes a comparator to compare (to examine carefully and critically, to examine (two or more objects, ideas, people, etc.) in order to note similarities and differences between contaminated and the control semiconductor, especially for flaws) the said two photoluminescence responses to

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determine the difference and obtain an indication of rates of diffusion so as to identify the contaminant ([pars. 0016, 0037, 0064-0068 and 0062], page 20, lines 9-11).

Higgs fails to explicitly specify a means to heat the sample in situ, allowing a photoluminescence response to be measured before and after heating.

Noguchi from the same field of endeavor teaches heating means (fig. 4: H) (col. 8, lines 27-32).

Therefore it would have been at least obvious to one having ordinary skill in the art at the time of invention to modify Higgs by means to heat the sample in situ for the purpose of controlling the temperature of the sample with accuracy.

As to claims 18 and 19, Higgs discloses the limitations that including imaging means (figs. 5: 25 and 29) to create an image map of the location of particulates on the surface of the semiconductor structure (fig. 5: 2); and wherein the imaging means generates a scattered light dark field and/or a reflected light image (figs. 1-4).

Additional Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The references listed in the attached form PTO-892 teach of other prior art method of detecting surface particulate defects, and especially metal particulates, in semiconductors such as silicon, to characterise defects likely to have an effect on the electrical activity of such semiconductor materials that may anticipate or obviate the claims of the applicant's invention.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Isiaka Akanbi whose telephone number is (571) 272-8658. The examiner can normally be reached on 8:00 a.m. - 4:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tarifur R. Chowdhury can be reached on (571) 272-2287. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Isiaka Akanbi

May 12, 2008

/TARIFUR R CHOWDHURY/ Supervisory Patent Examiner, Art Unit 2886